CLAIMS

What is claimed is:

1.   A system for determining a jitter tolerance of an optoelectronic device, comprising:

a generation circuit configured to generate a first sequence of bits and to transmit said first sequence of bits to a delay circuit configured to individually transmit bits in said first sequence to said optoelectronic device, each of said bits subject to a delay prior to being transmitted to said optoelectronic device; and

comparison circuitry configured to receive a second sequence of bits from said optoelectronic device, said second sequence of bits being derived by said optoelectronic device from said first sequence of bits;

wherein said comparison circuitry compares said second sequence of bits to said first sequence of bits and wherein said jitter tolerance of said optoelectronic device is determined by reference to said comparison.

2.   The system of claim 1, wherein said delay is changed by a predefined amount at a predefined frequency.

3.   The system of claim 1, wherein said delay is changed by a plurality of predefined amounts at a plurality of predefined frequencies.

4.   The system of claim 1, wherein the optoelectronic device is a transceiver.

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5.   The system of claim 1, wherein said generation circuit includes a bit sequence generator and a serializer/deserializer.

6.   The system of claim 1, wherein said comparison circuitry includes a controller that receives said first and second sequences of bits and compares said sequences to determine a number of bit errors, and wherein said number of bit errors is used to determine said jitter tolerance.

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7.   In a system for measuring a jitter tolerance of an optoelectronic device, said system being adapted to electrically communicate with the optoelectronic device and at least one master device, said system comprising a first bit sequence generator, a second bit sequence generator, a delay, and a controller, a method for computing the jitter tolerance comprising the steps of:

generating a first sequence of bits and transmitting said first sequence of bits to the delay;

delaying said first sequence of bits and individually transmitting said bits to the optoelectronic device;

transmitting a second sequence of bits from the optoelectronic device to the controller, said second sequence of bits derived by the optoelectronic device from the first sequence of bits;

comparing said first sequence of bits to said second sequence of bits to calculate a bit error rate; and

using said bit error rate to determine said jitter tolerance.

8.   The method of claim 7, wherein said delaying step includes delaying said bits by a predefined amount at a predefined frequency.

9.   The method of claim 7, wherein said delaying step includes delaying said bits by a plurality of predefined amounts at a plurality of predefined frequencies.

10.   The method of claim 7, wherein the optoelectronic device is a transceiver.

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11.   A system for determining a signal attenuation tolerance of an optoelectronic device, comprising:

a generation circuit configured to generate a first sequence of bits and to transmit said first sequence of bits to a delay circuit configured to individually transmit bits in said first sequence to an attenuator configured to perform an attenuation of a power level of said first sequence of bits by a predefined amount and to then transmit said first sequence of bits to the optoelectronic device; and

comparison circuitry configured to receive a second sequence of bits from the optoelectronic device, said second sequence of bits being derived by the optoelectronic device from said first sequence of bits;

wherein said comparison circuitry compares said second sequence of bits to said first sequence of bits and wherein said signal attenuation tolerance of said optoelectronic device is determined by reference to said comparison.

12.   The system of claim 11, wherein said comparison circuitry includes a controller that receives said first and second sequences of bits and compares said sequences to determine a number of bit errors, and wherein said number of bit errors is used to determine said attenuation tolerance.

13.   The system of claim 12, wherein said delay is changed by a predefined amount at a predefined frequency.

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14.   The system of claim 13, wherein said attenuator is configured to attenuate said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by said predefined amount at said predefined frequency, and said bit error rate is calculated for each of said attenuation levels, said bit error rates being combined to determine said attenuation tolerance.

15.   The system of claim 12, wherein said delay is changed by a plurality of predefined amounts at a plurality of predefined frequencies.

16.   The system of claim 15, wherein said attenuator is configured to attenuate said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by each of said predefined amounts at each of said predefined frequencies to form a plurality of data points, and said bit error rate is calculated for each of said plurality of data points, said bit error rates for each of said plurality of data points being combined to determine said attenuation tolerance.

17.   The system of claim 11, wherein said optoelectronic device is a transceiver.

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18.   In a system for measuring an attenuation tolerance of an optoelectronic device, said system being adapted to electrically communicate with the optoelectronic device and an optical attenuator, said system comprising a first bit sequence generator, a second bit sequence generator, a delay, and a controller, a method for computing the attenuation tolerance comprising the steps of:

generating a first sequence of bits and transmitting said first sequence of bits to the delay;

delaying said first sequence of bits and individually transmitting said bits to the optoelectronic device;

transmitting a second sequence of bits from the optoelectronic device to the optical attenuator, said second sequence of bits derived by the optoelectronic device from the first sequence of bits;

attenuating a power level of said second sequence of bits and transmitting said first sequence of bits and said second sequence of bits to the controller;

comparing said first sequence of bits to said second sequence of bits to calculate a bit error rate; and

using said bit error rate to determine said attenuation tolerance.

19.   The method of claim 18, wherein said delaying step includes delaying said first sequence of bits by a predefined amount at a predefined frequency.

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20.   The method of claim 19, wherein said attenuating step includes attenuating said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by said predefined amount at said predefined frequency, and said bit error rate is calculated for each of said attenuation levels, said bit error rates being combined to determine said attenuation tolerance.

21.   The method of claim 18, wherein said delaying step includes delaying said first sequence of bits by a plurality of predefined amounts at a plurality of predefined frequencies.

22.   The method of claim 21, wherein said attenuating step includes attenuating said power level at a plurality of attenuation levels, and wherein, for each attenuation level, said delay is changed by each of said predefined amounts at each of said predefined frequencies to form a plurality of data points, and said bit error rate is calculated for each of said plurality of data points, said bit error rates for each of said plurality of data points being combined to determine said attenuation tolerance.

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